In the Claims:

Please amend claim 22. The claims are as follows:

1. - 10. (Canceled)

11. (Previously Presented) A method of fabricating a filled trench structure, comprising:

(a) forming a planarization stop layer on a top surface of a substrate;

(b) forming a first set of trenches in a first region of said planarization stop layer and said substrate and forming a second set of trenches in a second region of said planarization stop layer and said substrate, trenches in said first set of trenches having a higher aspect ratio than said trenches in said second region;

(c) depositing a layer of a fill material in and over said first and second sets of trenches and on a top surface of said planarization stop layer, said fill material completely filling each trench of said first set of trenches and completely filling each trench of said second sets of trenches, a first thickness of said layer of said fill material directly over each trench of said first set of trenches greater than a second thickness of said layer of said fill material directly over each trench of said second set of trenches, said first and second thicknesses measured perpendicularly from a plane coplanar with said top surface of said planarization stop layer to a top surface of said layer of said fill material;

(d) after (c), non-selectively removing, using a non-planarization process, an entire uppermost layer of said fill material from over said first and second regions and said top surface of said planarization stop layer to form a thinned layer of said fill material over said first and second regions and on said top surface of said planarization stop layer, said fill material still

completely filling each trench of said first set of trenches and each trench of said second set of trenches; and

(e) after (d), removing using a planarization process, all said thinned layer of said fill material from said top surface of said planarization stop layer and over said first and second regions, said fill material still completely filling each trench of said first set of trenches and each trench of said second set of trenches, a top surface of said fill material in said first set of trenches and a top surface of said fill material in said second sets of trenches co-planer with said top surface of said planarization stop layer.

12. (Canceled)

13. (Previously Presented) The method of claim 11, wherein in (e) said planarization process includes chemical-mechanical polishing or fixed abrasive grinding.

14. (Canceled)

15. (Previously Presented) The method of claim 11, wherein (d) removes about 5 to 20% of an as deposited thickness of said fill material.

16. (Original) The method of claim 11, wherein the aspect ratio of trenches in said first set of trenches is greater than about 3:1 and the aspect ratio of trenches in said second region is less than about 3:1.

17. (Original) The method of claim 11, wherein said first region is a memory cell array region and said second region is a support circuit region of an integrated circuit.

18. (Original) The method of claim 11, wherein said fill material is selected from the group consisting of: high-density plasma oxide, low-pressure chemical vapor deposition oxide, tetraethoxysilane oxide, silicon nitride, bis(tertiary-butylamine)silane, a thin layer of conformal insulator and a fill layer of N-doped, P-doped or un-doped polysilicon, tungsten, copper or aluminum.

19. (Previously Presented) The method of claim 22, wherein after (d) and before (e), a first volume of fill material in said first region not completely contained in said trenches of said first set of trenches is about equal to a second volume of fill material in said second region not completely contained in said trenches of said second set of trenches.

20. (Previously Presented) The method of claim 22, wherein (d) removes about 5 to 20% of the as deposited thickness of said fill material.

21. (Previously Presented) The method of claim 22, wherein (d) reduces the difference between a volume of said fill material over first region and a volume of said fill material over said second region.

22. (Currently Amended) A method of fabricating a filled trench structure, comprising:

(a) forming a planarization stop layer on a top surface of a substrate;

(b) forming a first set of trenches in a first region of said planarization stop layer and said substrate and forming a second set of trenches in a second region of said planarization stop layer and said substrate, trenches in said first set of trenches having a higher aspect ratio than said trenches in said second region;

(c) depositing a layer of a fill material in and over said first and second sets of trenches and on a top surface of said planarization stop layer, said fill material completely filling each trench of said first set of trenches and completely filling each trench of said second sets of trenches;

(d), after (c):

(i) forming a mask layer on said layer of fill material;

(ii) forming a opening in said mask layer in said first region and over trenches of said first set of trenches;

(iii) removing a layer of said layer of said fill material exposed in said opening, said fill material still completely filling each trench of said first set of trenches, after said removing of said layer of said layer of said fill material, said fill layer of material thicker over said planarization stop layer between adjacent trenches of said first set of trenches then over said fill material contained within each trench of said first set of trenches; and

(iv) removing said masking layer; and

(e) after (d), removing, using a planarization process, all of said layer of said fill material from said top surface of said planarization stop layer and over said first and second regions, said fill material still completely filling each trench of said first set of trenches and each trench of said second set of trenches, a top surface of said fill material in said first set of trenches and a top

surface of said fill material in said second sets of trenches co-planer with said top surface of said planarization stop layer.

23. (Previously Presented) The method of claim 22, wherein (d) includes a wet etching, a dry etching, a reactive ion etching or a plasma etching process.

24. (Previously Presented) The method of claim 22, wherein in (e) said planarization process includes chemical-mechanical polishing or fixed abrasive grinding.

25. (Previously Presented) The method of claim 11, wherein in (d) said non-planarization process includes a wet etching, a dry etching, a reactive ion etching or a plasma etching process.

26. (Previously Presented) The method of claim 11, wherein in (d), after said removing, a third thickness of said thinned layer of said fill material directly over each trench of said first set of trenches is greater than a fourth thickness of said thinned layer of fill material directly over each trench of said second set of trenches, said third and fourth thicknesses measured perpendicularly from a plane coplanar with said top surface of said planarization stop layer to a top surface of said thinned layer of fill material.

27. (Previously Presented) The method of claim 22, wherein in (c) after said depositing, a first thickness of said layer of said fill material directly over each trench of said first set of trenches is greater than a second thickness of said layer of said fill material directly over each trench of said second set of trenches, said first and second thicknesses measured perpendicularly from a plane

coplanar with said top surface of said planarization stop layer to a top surface of said layer of said fill material.

28. (Previously Presented) The method of claim 22, wherein the aspect ratio of trenches in said first set of trenches is greater than about 3:1 and the aspect ratio of trenches in said second region is less than about 3:1.

29. (Previously Presented) The method of claim 22, wherein said first region is a memory cell array region and said second region is a support circuit region of an integrated circuit.

30. (Previously Presented) The method of claim 22, wherein said fill material is selected from the group consisting of: high-density plasma oxide, low-pressure chemical vapor deposition oxide, tetraethoxysilane oxide, silicon nitride, bis(tertiary-butylamine)silane, a thin layer of conformal insulator and a fill layer of N-doped, P-doped or un-doped polysilicon, tungsten, copper or aluminum.